M2816A
Timer E²
16K Electrical Erasable ROMs

August 1985

Features

- **High Endurance Write Cycles**
  - **2816A: 10,000 Cycles/Byte**
- **On-Chip Timer**
  - **Automatic Erase and Write Time Out**
- **All Inputs Latched by Write or Chip Enable**
- **Direct Replacement to 2K x 8 E²ROMs**
  - **21 V 2816**
  - **5 V Timer 2816A**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Low Power Operation**
  - **110 mA max. Active Current**
  - **40 mA max. Standby Current**
- **JEDEC Approved Byte-Wide Pinout**

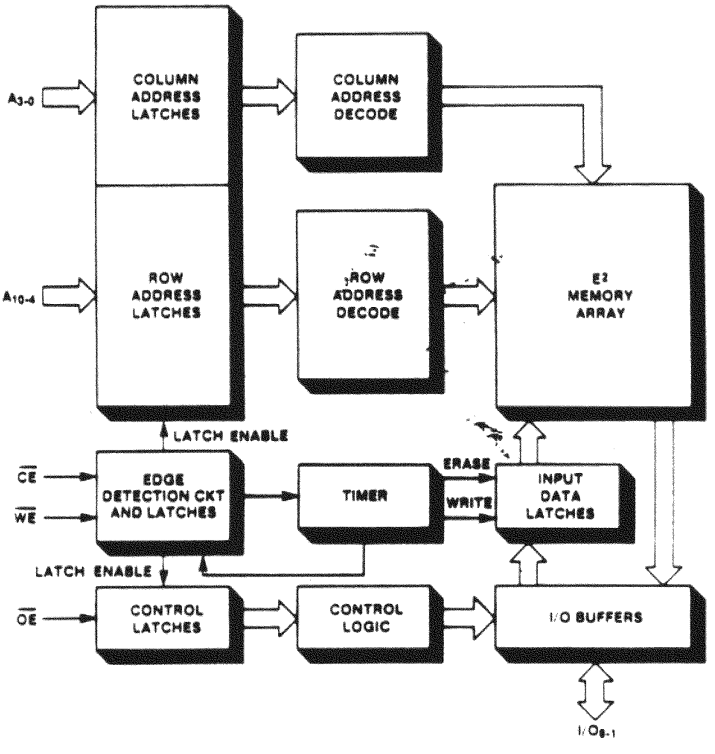
Description

SEEQ's M2816A is a 5 V only, 2K x 8 electrically erasable read only memory (E²ROM). E²ROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times that a byte may be written, is 10 thousand for the M2816A. The M2816A's high endurance was accomplished using SEEQ's proprietary oxynitride E²ROM process and its innovative "Q cell™" design. The M2816A is ideal for systems that require frequent updates.

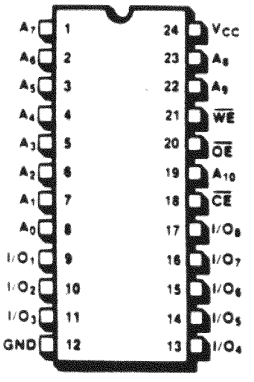
There is an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable ($\overline{WE}$) pulse width needs to be only 150 ns. The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the microcomputer system

(continued on next page)

Block Diagram



Pin Configuration



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

for other tasks during the write time. The M2816A's write time is 10 ms. Once a byte is written, it can be read in 250 ns. The inputs are TTL for both the byte write and read mode.

The E²ROM is ideal for systems with limited board area. For systems where cost is important or higher density is required, SEEQ has a latch only "52B" family at 16K and 64K bit densities. The "52B" family has the same JEDEC approved pin configuration but without the on-chip timer. All "52B" family inputs are latched by the falling edge of the write enable signal.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of $\overline{CE}$ or $\overline{WE}$ and data is latched on the first rising edge of $\overline{CE}$ or $\overline{WE}$. An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode.

The chip erase mode clears all data to a TTL high in one 9 ms cycle. This is accomplished by raising both $\overline{WE}$ and $\overline{OE}$ to a high voltage (e.g. 21 V) and having all the data inputs at a TTL high. In addition an optional 21 V byte write (preceded by a byte erase) mode is available.

Mode Selection (Table 1)

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}*	D_{IN}
Write or Read Inhibit	V_{IL}	V_{IH}	V_{IH}	High Z
Chip Erase	V_{IL}	V_{ER}	V_{ER}	V_{IH}

*A 21 V input on $\overline{WE}$ is an optional mode.

Power Up/Down Considerations

The 2816A/5516A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... -65° C to +150° C
Under Bias ..... -65° C to +135° C

All Inputs or Outputs with Respect to Ground ..... +6V to −0.3V

$\overline{WE}$ During Writing/Erasing with Respect to Ground ..... +22.5V to −0.3V

Duration of $\overline{WE}$ Supply at 22V During W/E Inhibit ..... 24 Hours

Recommended Operating Conditions

Temperature Range: ..... -55° C to +125° C
V_{CC} Power Supply: ..... 5V ±10%
Q (Maximum Endurance/Byte): ..... 10,000 cycles

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Operating Characteristics (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active Vcc Current		125	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; All I/O Open; Other Inputs = 5.5 V
I_{SB}	Standby Vcc Current		40	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}; All I/O's Open; Other Inputs = 5.5 V
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 5.5 V
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = 5.5 V
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA
V_{ER}	$\overline{OE}$ and $\overline{WE}$ Voltage in Chip Erase Mode	12	22	V	I_{ER} = 10 μA

AC Characteristics (Over the operating V_{CC} and temperature range)

Read Operation

Symbol	Parameter	Limits (ns)				Units
		M2816A-250		M2816A-350		
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		350		ns
t_{CE}	Chip Enable Access Time		250		350	ns
t_{AA}	Address Access Time		250		350	ns
t_{OE}	Output Enable Access Time		90		100	ns
t_{LZ}	$\overline{CE}$ to Output in Low Z	10		10		ns
t_{HZ}	$\overline{CE}$to Output in High Z	10	100	10	100	ns
t_{OLZ}	$\overline{OE}$ to Output in Low Z	50		50		ns
t_{OHZ}	$\overline{OE}$ to Output in High Z	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	50		50		ns
t_{PU}	$\overline{CE}$ to Power-up Time	0		0		ns
t_{PD}	$\overline{CE}$ to Power Down Time		50		50	ns

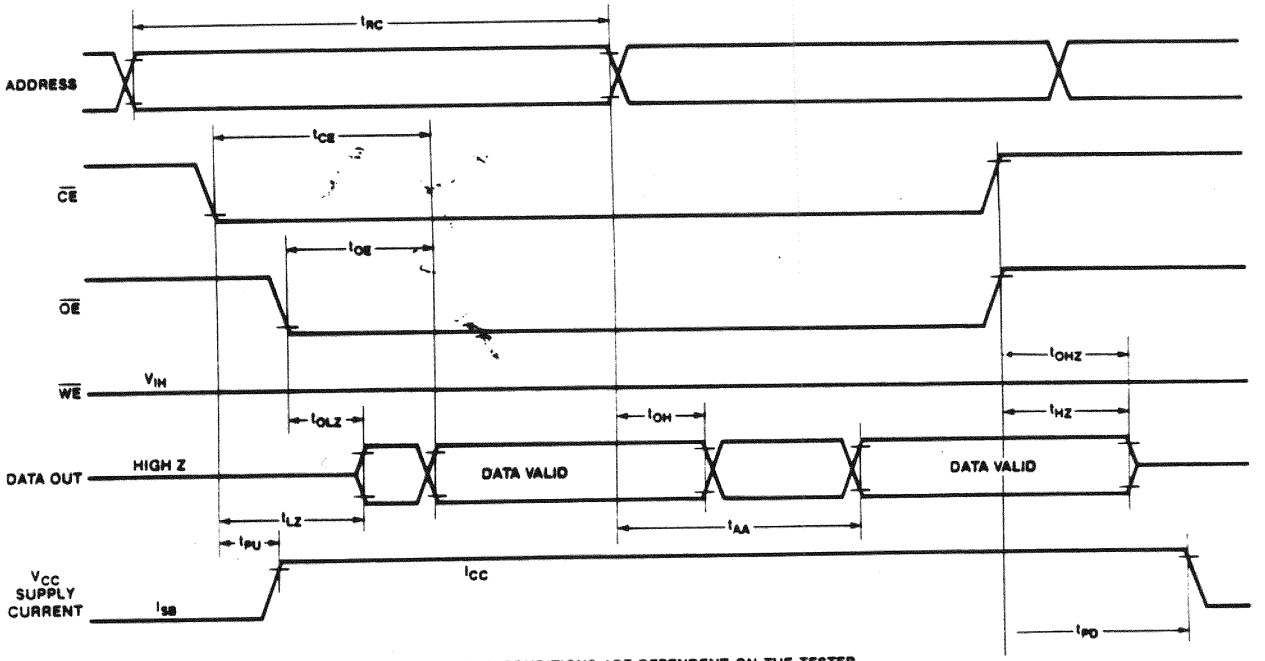
Capacitance T_A = 25° C, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = 0 V
C_{OUT}	Data (I/O) Cap.	10 pF	$V_{I/O}$ = 0 V

Equivalent A.C. Test Conditions[1]

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

READ CYCLE TIMING



NOTE 1: THIS IS AN EQUIVALENT TEST CONDITION AND ACTUAL CONDITIONS ARE DEPENDENT ON THE TESTER.

AC Characteristics (Over the operating V_{CC} and temperature range)

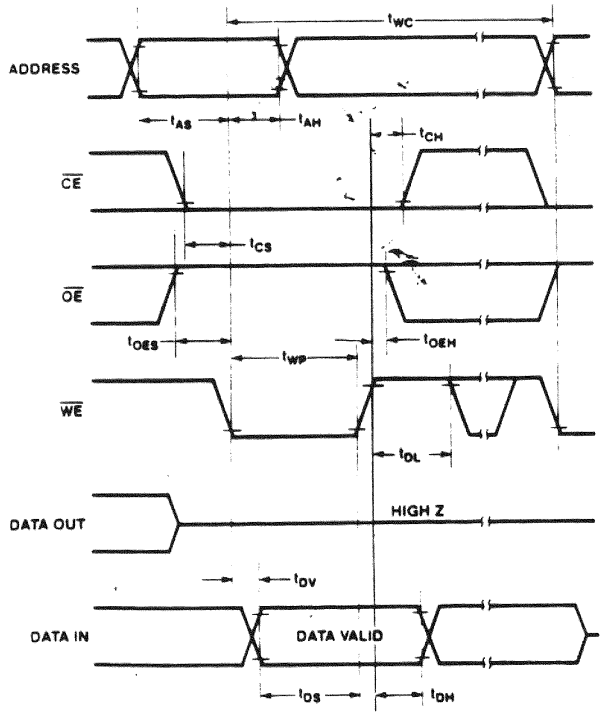
TTL WRITE CYCLE

Symbol	Parameter	Limits (ns)				Units
		M2816A-250		M2816A-350		
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	10		10		ms
t_{AS}	Address Set Up Time	10		10		ns
t_{AH}	Address Hold Time	50		70		ns
t_{CS}	Write Set Up Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CW}	$\overline{CE}$ to End of Write Input	150		150		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		ns
t_{WP}[1]	$\overline{WE}$ Write Pulse Width	150		150		ns
t_{DL}	Data Latch Time	50		50		ns
t_{DV}[2]	Data Valid Time		1		1	μs
t_{DS}	Data Set Up Time	20		50		ns
t_{DH}	Data Hold Time	20		20		ns

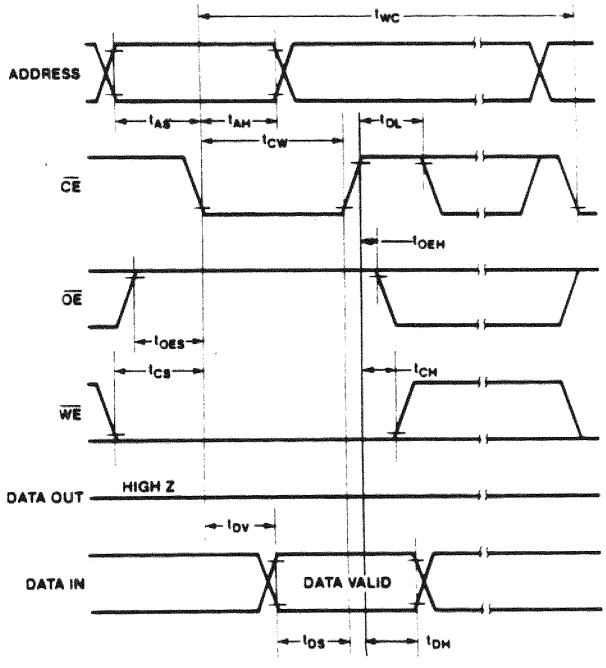
Notes:
1. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 μs maximum after the initiation of a write cycle.

TTL Byte Write Cycle

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE

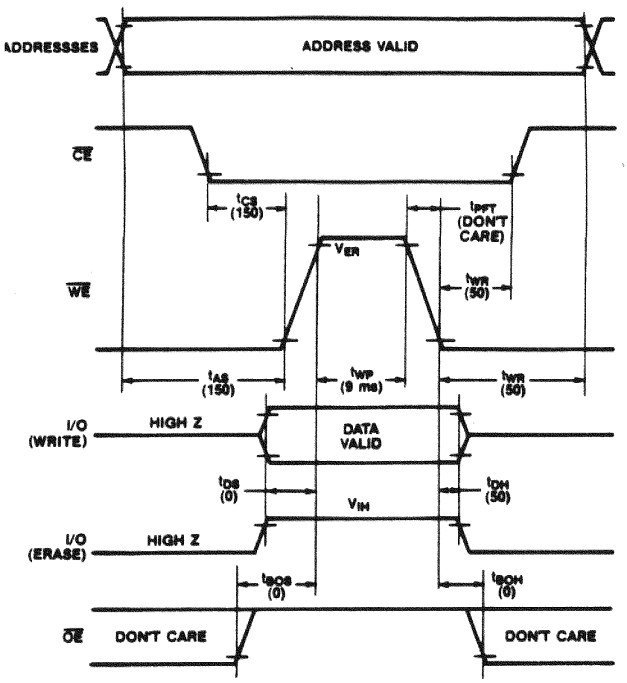


AC Characteristics

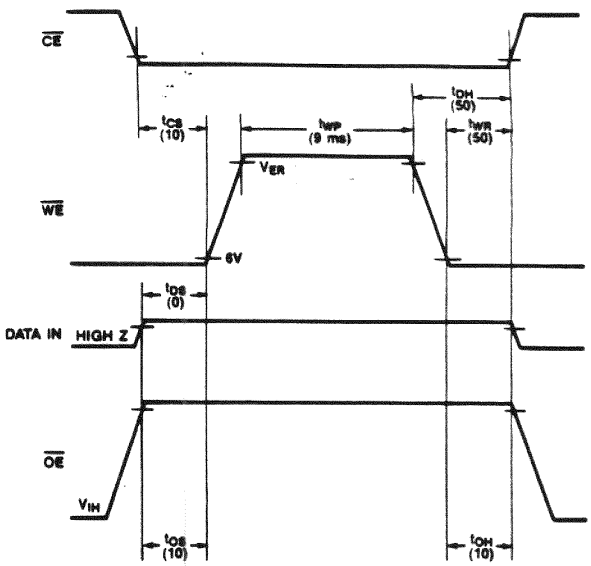
21 V Optional Erase or Write Cycle

(All times shown in parentheses are in ns and are minimum value, unless otherwise noted.)

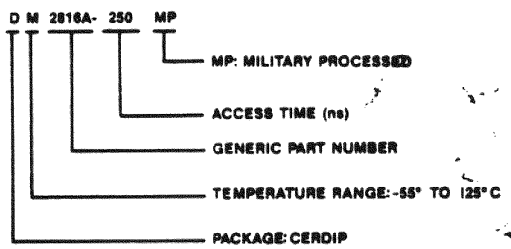
21 V BYTE ERASE OR BYTE WRITE TIMING



21 V CHIP ERASE CYCLE

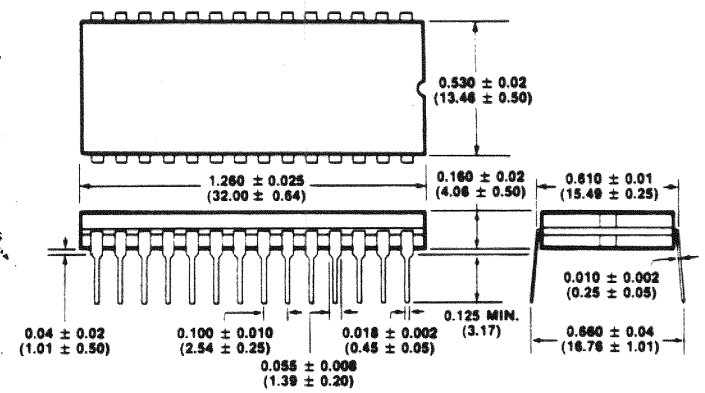


Ordering Information



Package Diagram

24-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).